a logic circuit that carries out logical operations on the output signal of the delay adjustment circuit according to claim 2, and outputs a clock having an operational frequency N times said reference clock.

13. A clock generating circuit comprising:

the delay adjustment circuit according to claim 3 into which a reference clock is input; and

a logic circuit that carries out logical operations on the output signal of the delay adjustment circuit according to claim 3, and outputs a clock having an operational frequency N times said reference clock.

14. A clock generating circuit comprising:

the delay adjustment circuit described in claim 2 into which a reference clock is input;

logic circuit that carries out logical operation on a reference clock and the output signal of the delay adjustment circuit according to claim 2 and outputs a clock having an operational frequency N times that of said reference clock; and

a setting device that fixes the output of the delay adjustment circuit according to claim 2 to a constant value only during the non-operational mode; and

wherein a clock is output that has an operational frequency that is equal to that of the reference clock when serving as the non-operational mode or N times the reference clock when serving as the operational mode based on the result of the logical processing of said logic circuit.

15. A clock generating circuit comprising:

the delay adjustment circuit described in claim 3 into which a reference clock is input;

logic circuit that carries out logical operation on a reference clock and the output signal of the delay adjustment circuit according to claim 3 and outputs a clock having an operational frequency N times that of said reference clock; and

a setting device that fixes the output of the delay adjustment circuit according to claim 3 to a constant value only during the non-operational mode; and